Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A technique for testability of a semiconductor integrated circuit, comprising:

the first step of conducting a fault simulation for the semiconductor integrated circuit based on a set of predetermined test ~~pattern~~ signals and corresponding test results, and discriminating a detectable fault and an undetectable fault from each other, the predetermined test signals being a set of output values from a plurality of registers at an input side of a test object in the semiconductor integrated circuit

the second step of [[list]] listing undetectable faults as undetected faults;

the third step of determining [[the]] test signals ~~conditions~~ for ~~testing~~ detecting the undetected faults;

the fourth step of determining [[a]] test signals ~~pattern~~ most likely to meet the test signals ~~conditions~~ of the third step from among the set of predetermined test signals ~~patterns~~ of the fault simulation of the first step;

the fifth step of replacing registers at the input side associated with the undetected faults of the second step with scan registers and connecting the scan registers in a scan chain thereby to construct a modified circuit; and

the sixth step of conducting the fault simulation or [[the]] a test by switching to the test signals ~~condition~~ determined in the ~~third~~ fourth step at the timing corresponding to the undetected faults while using the ~~determined~~ predetermined test signals ~~pattern~~ in the ~~fourth~~ first

step for the modified circuit.

2. (Original) A technique for testability of a semiconductor integrated circuit according to claim 1, wherein the fifth step includes the step of replacing the input-side registers associated with the undetected faults not by scan registers but by registers with set or reset function thereby to constitute a modified circuit.

3. (Currently Amended) A technique for testability of a semiconductor integrated circuit, wherein [[the]] registers connected to a combination logic circuit constituting an object of [[the]] a test in the semiconductor integrated circuit are classified into first registers that can be controlled and observed directly from a built-in processor, second registers that can be controlled and observed directly from a terminal of the semiconductor integrated circuit and third registers other than the first and second registers, the technique comprising:

the first step of replacing the third registers with scan registers and connecting the scan registers in a scan chain to thereby constitute a modified circuit;

the second step of setting and inputting [[the]] test data to the first and second registers from selected one of the processor and the integrated circuit terminal;

the third step of setting and inputting [[the]] test data to the third register with the shift operation through the scan chain;

the fourth step of performing [[the]] a capture operation of the test data for the combination logic circuit;

the fifth step of outputting [[the]] test result data from the third register with the shift operation through the scan chain; and

the sixth step of outputting [[the]] test result data from the first and second registers.

4. (New) A technique for testability of a semiconductor integrated circuit according to claim 1, wherein the fourth step is conducted by comparing each signal constituting the test signals of the third step to a corresponding signal constituting the predetermined test signals.

5. (New) A technique for testability of a semiconductor integrated circuit according to claim 4, wherein the registers associated with the undetected faults are registers on the input side outputting a different signal from the corresponding signal constituting the predetermined signals.